SRL TECHNICAL REPORT 76-1

MJS CRS

Science Requirements Document

28 Jan 1976

Tom Garrard

Revised 25 Feb 1976

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Voyager

SRD

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JHT	Jim Trainor		663	6282	

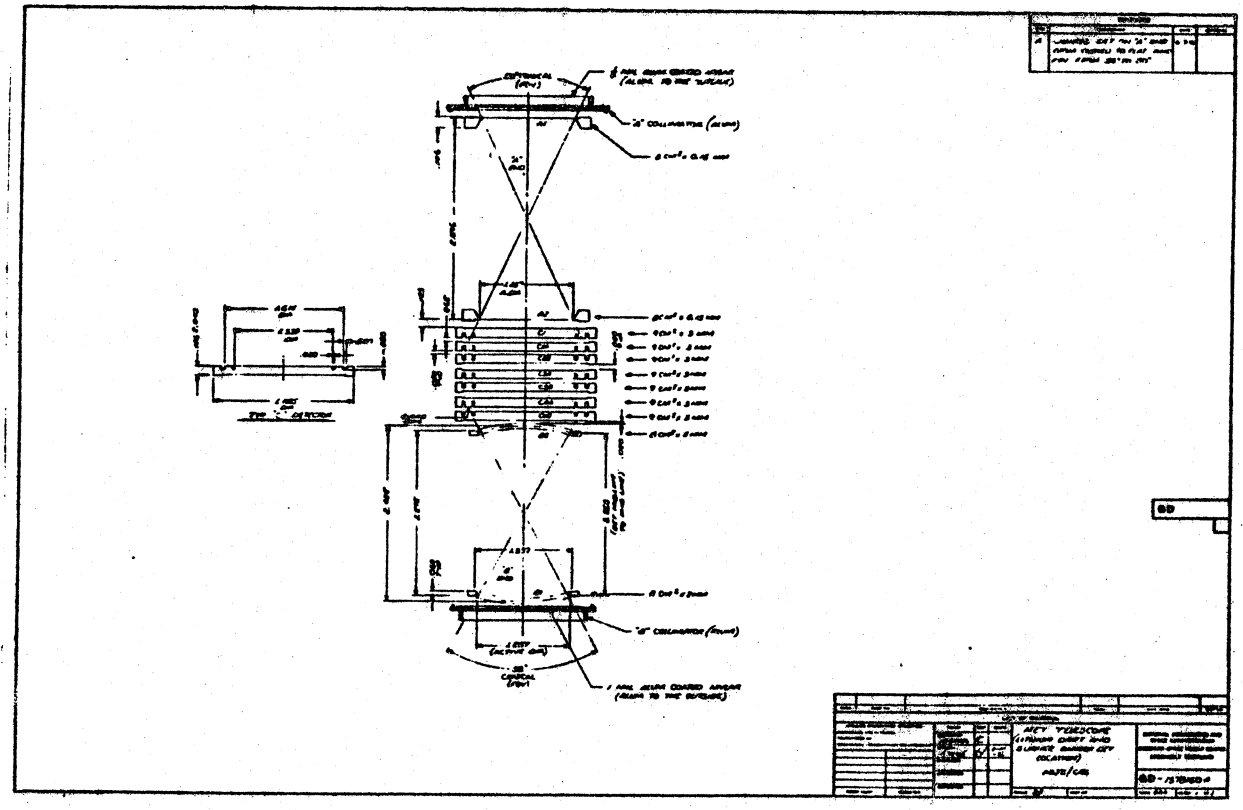
1/28/76 : So many changes since the 2/24/75 issue that I won't even try to list them. This entire document should be carefully studied.

2/25/76 : Changes and additions as discussed in the CRS team meeting of 16 and 17 Feb 1976.

8/25/76 : New HET config. Gain disc values are nominal design goals. Actual values will be listed when they are reported. HET guard logic modified. THI typo corrected on page 19. Block diagram added. Description of tag bits made more explicit. Typo corrected in equations for R5, R6, R7 on page 25. Cal stim modified.

4/01/77 : Swap SB, SB* in R5, R6, R7 on pages 9, 24, 27. Change L1, L2, L4 thresholds on page 11. G2* in HET tag word on page 23. Typo in LET SL* equation on page 24. Distinguish HG1 and HG2 on page 25. Correct missing D8* term in R28 on page 26. Add page 28,29. Modify analog mux list on page 33.

1) Telescope Schematic



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design goals :

Detector	High Gain thresh (MeV)	High Gain full scale (MeV)	High Gain channel width (keV)	Low Gain thresh (MeV)	Low Gain full scale (GeV)	Low Gain channel width (MeV)	gain change factor
A1,A2	0.1	188	46	0.5	0.94	0.23	5.
B1	0.3	730	178	1.02	2.50	0.61	3.42
B2	0.3	730	178	2.04	5.00	1.22	6.84
C1	0.5	1024	250	2.5	5.12	1.25	5.
C2, C3, C4	0.92	XX	XX	4.6	XX	XX	5.
C1 + C2 + C3	XX	3523	860	XX	17.61	4.30	5.
C2 + C3 + C4	XX	3523	860	XX	17.61	4.30	5.
G1	0.3	XX	XX	0.3	XX	XX	XX
G2	2.5	XX	XX	2.5	XX	XX	XX
G3	9.	XX	XX	9.	XX	XX	XX

$0.3\ \text{MeV} \times \frac{10^4\ \text{mV}}{396\ \text{MeV}} = 7.6\ \text{mV}$

$2.5\ \text{MeV} \times$ " $= 63.1$ "

9.0 " $\times$ " $= 227$ "

G1:G2:G3 = 1:8.33:30

Slants

SB :
B1 + B2 + (C1 + C2 + C3) = 60 (channels)
Low Gain B1 + 0.5B2 + 0.142(C2 + C3 + C4) = 36.6 (Mev)
High Gain B1 + B2 + 0.207(C2 + C3 + C4) = 10.7 (MeV)

SA : Low Gain only
SA2 : A1 + 0.60A2 + 0.29(C1 + C2 + C3) = 24 (MeV)
SA1 : A1 + 0.60A2 + 0.02(C1 + C2 + C3) = 9 (MeV)
SA = SA1.SA2

Full Scale = 10V in preamp, 5v in ADC; coupling done with 2:1 transformer.
G1, G2, G3: 10V preamp output for 396 MeV, not gain switched.
C2, C3, C4: 10V preamp output for 1.86 GeV in high gain, 9.63 GeV in low gain.

$\frac{9.63}{1.88} = 5.18$!

$\frac{1.86}{3.523} \times 4096 \rightarrow 2163$

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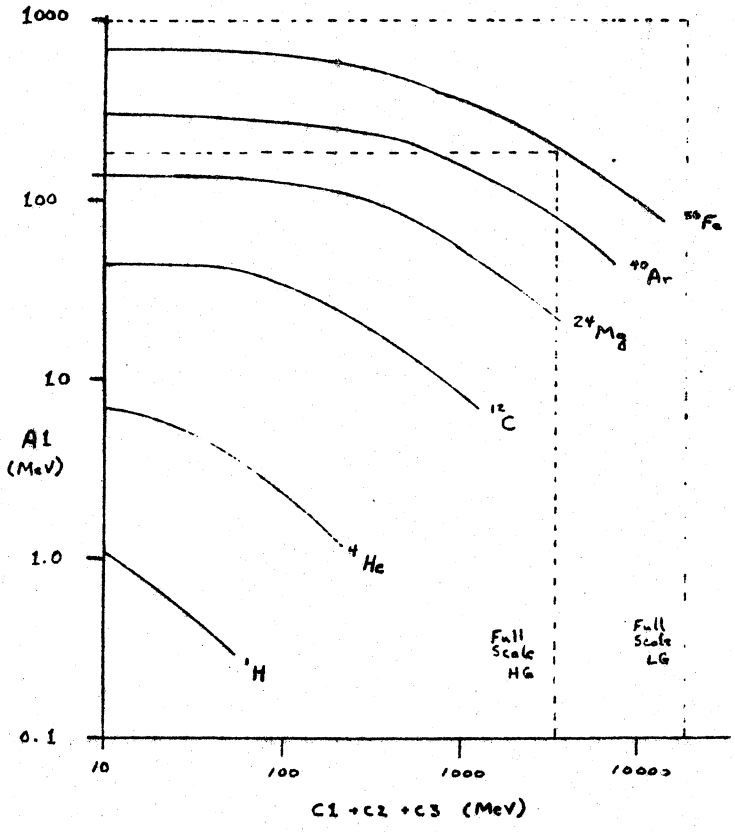
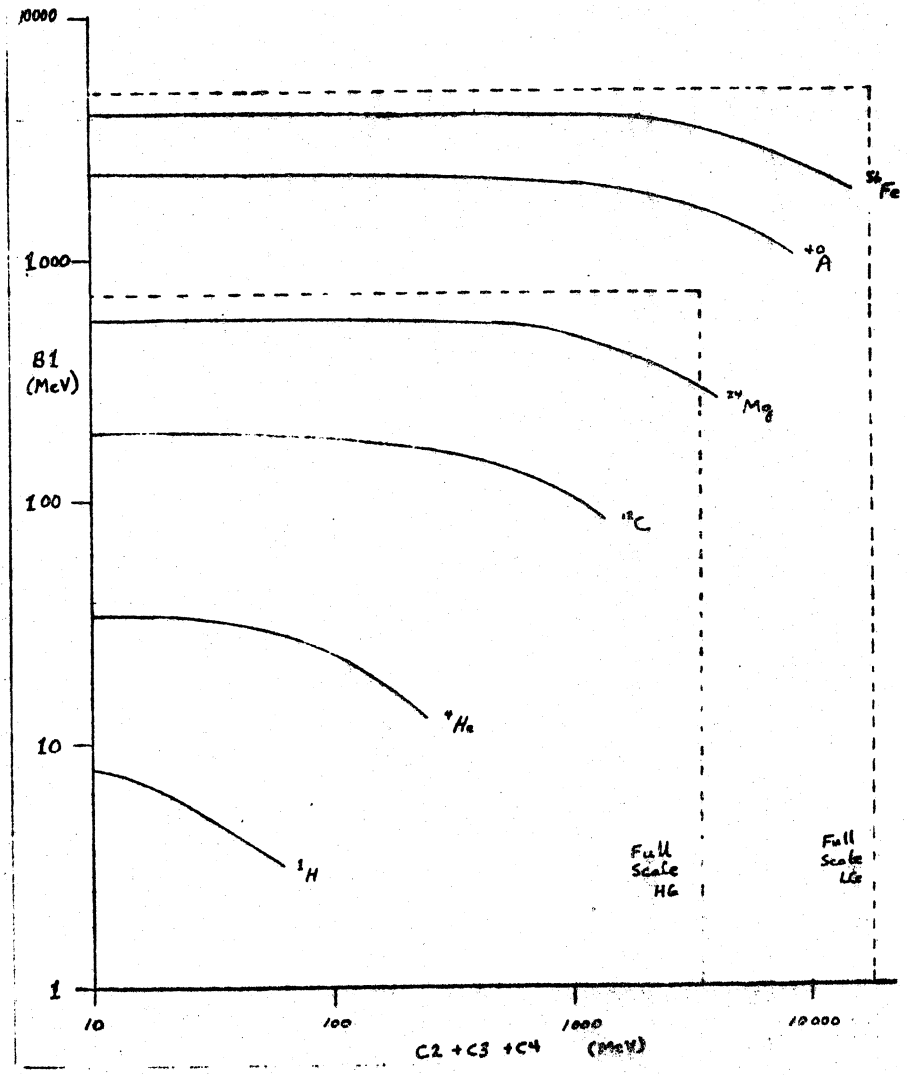
HET 3) Delta E vs E' Plots





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Event Type	Range	Geometry Factor (cm**2.sr)
AS	A2	??
AS	C3	??
BS	B2	1.67
BS	C2	0.793
PEN		??

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HET 1 is described; HET 2 is similar.

Name	Accum Number	Gain (S5)	Subcom State (S1 - S4)	Simplified Logic Equation	Description
AS	R1	HG	all	A1.A2.C4*.G1*	All nuclei of appropriate range, 0.15 to 15.3 mm Si nominal. Electrons eliminated by thin A detectors.
ASZ3	R1	LG	all	A1.A2.SA.C4*.G3*	All nuclei of Z>=3 of appropriate range, 0.15 to 15.3 mm Si nominal. Z<3 eliminated by slant, SA.
BSZ2	R2	LG	all	B1.B2.SB.C1*.G3*	All nuclei of Z>=2 of appropriate range, 2 to 22 mm Si nominal. Electrons, Z=1 eliminated by slant, SB.
BSp	R2	HG	S1=0 or S2=0(3/4)	B1.B2.SB.C1*.G1*	All nuclei of appropriate range, 2 to 22 mm Si nominal.
BSe	R2	HG	S1=S2=1 (1/4)	B1.B2.C4.SB*.C1*.G1*	Electrons of appropriate range, 4 to 22 mm Si nominal. Nuclei eliminated by slants.
PEN	R3	both	all	B1.B2.C1	All particles of range greater than 22 mm Si nominal.
PG	R4	both	all	PEN.G1*	Same as PEN, but some heavies lost due to knock-ons and cross-talk in guards.
BS4Z2*	R5	LG	odd (S1=1)	B1.B2.C4.C3*.SB*.G1*	Protons of appropriate range, 4 to 10 mm. Z>=2 eliminated by slant. Most electrons eliminated by high thresholds on B1 and B2.
BS4Z2	R5	LG	even (S1=0)	B1.B2.C4.C3*.SB.G1*	Z>=2 of appropriate range, 4 to 10 mm.
BS4e	R5	HG	odd	B1.B2.C4.C3*.SB*.G1*	Electrons of 4 to 10 mm. Nuclei eliminated by slant.
BS4p	R5	HG	even	B1.B2.C4.C3*.SB.G1*	Nuclei of 4 to 10 mm. Electrons eliminated by slant.
BS3Z2*	R6	as above		- - C4.C3.C2* - -	As above, except nominal range of 10 to 16 mm Si.
BS3Z2					
BS3e					
BS3p					
BS2Z2*	R7	as above		- - C4.C3.C2.C1* - -	As above, except nominal range of 16 to 22 mm Si.
BS2Z2					
BS2e					
BS2p					

Analysis is tied to rates R1, R2, and R3. Buffers are called HET AS, HET BS, and HET P.
Following table shows name of analysis requirement as function of gain, subcom state, and buffer.

Buffer		HET AS	HET BS	HET P
Gain	Subcom State			
LG	all	ASZ3	BSZ2	PEN
HG	S1=0 or S2=0	AS	BSp	PEN
HG	S1=S2=1	AS	BSe	PEN

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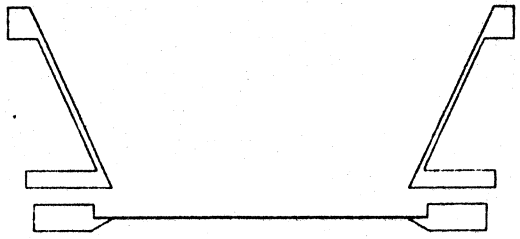

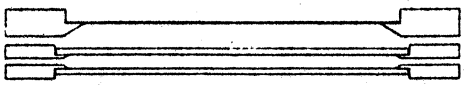

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Detector	Threshold (MeV)	Full Scale (MeV)	Channel Width (keV)
L1, L2	0.2	307	75
L3	1.00	2048	500
L4	0.3	XX	XX

Slant
SL : L1 + 0.42L2 + 0.20L3 = 9.6 (MeV)

Discriminators :

Temperature Drift	<= 1%	-25C to 15C
Initial Setting	+- 3%	
Adjustability	+-15%	

L4: 10V preamp output for 25 MeV.
2:1 transformer is on output of L4 preamp.

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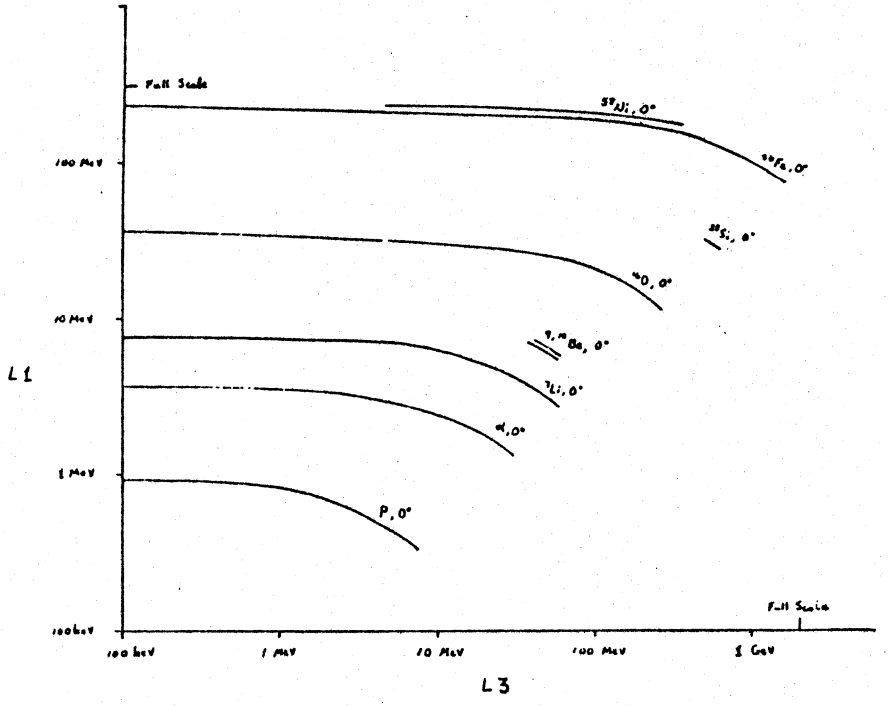

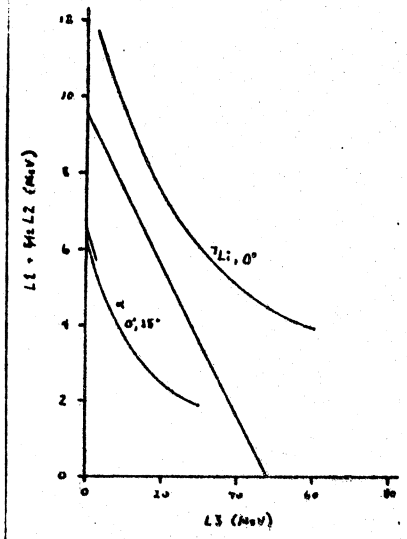

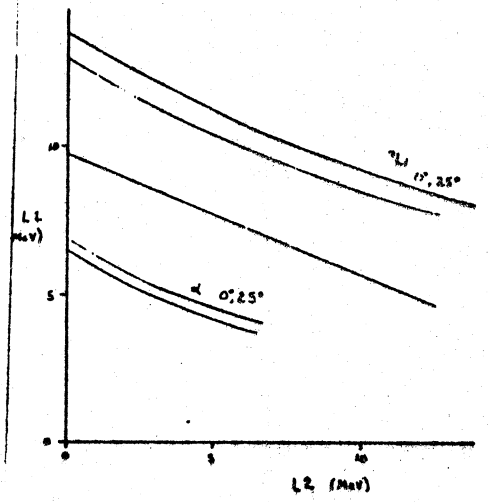

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Nominal LET geometry factor is 0.44 cm**2-sr.

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LET A is described; LET's B, C, and D are similar.

Name	Accum Number	Subcom State (S1-S4)	Simplified Logic Equation	Description
LAZ3*	R17	all	L1.L2.L3.SL*.L4*	Z<3 of appropriate range, 70 to 520 microns Si nominal.
LAZ3	R18	all	L1.L2.L3.SL.L4*	Z>=3 of appropriate range, 70 to 520 microns Si nominal.
LATRP	R25	6 & 14	L1.L2.L3.L4*	Nuclei of appropriate range, 70 to 520 microns Si nominal.

LAZ3* causes analysis and events are stored in buffer LET SL*.
LAZ3 causes analysis and events are stored in buffer LET SL.

Note that R17 and R18 are subject to modification by the command system; R25 is not.

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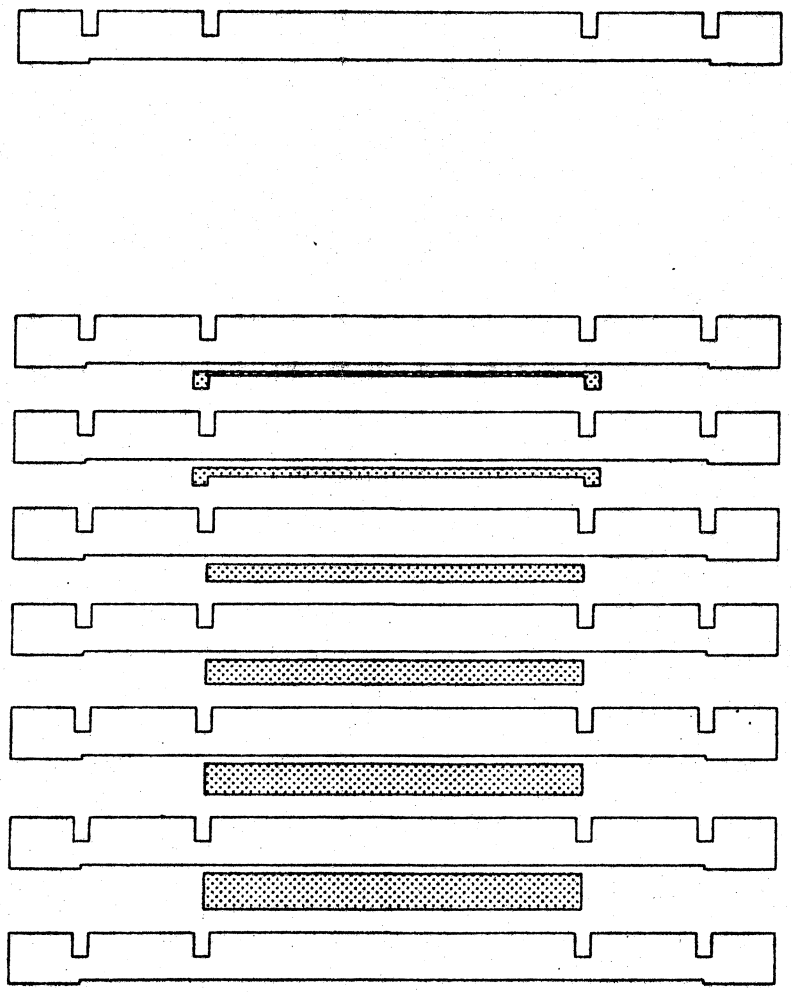

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Detector	Threshold Lower (MeV)	Threshold Upper (MeV)	Full Scale (MeV)	Channel Width (keV)
D1, D2	0.5	2.5	2.5	19.4
D3 to D7	0.5	8.0	XX	XX
D8	0.2	XX	XX	XX
GA, GB	0.2	XX	XX	XX

Discriminators :
D3H to D7H Adjustability +-25%

Preamp full scale 10V = 24.70 MeV
2.47 MeV = channel 127 of ADC.

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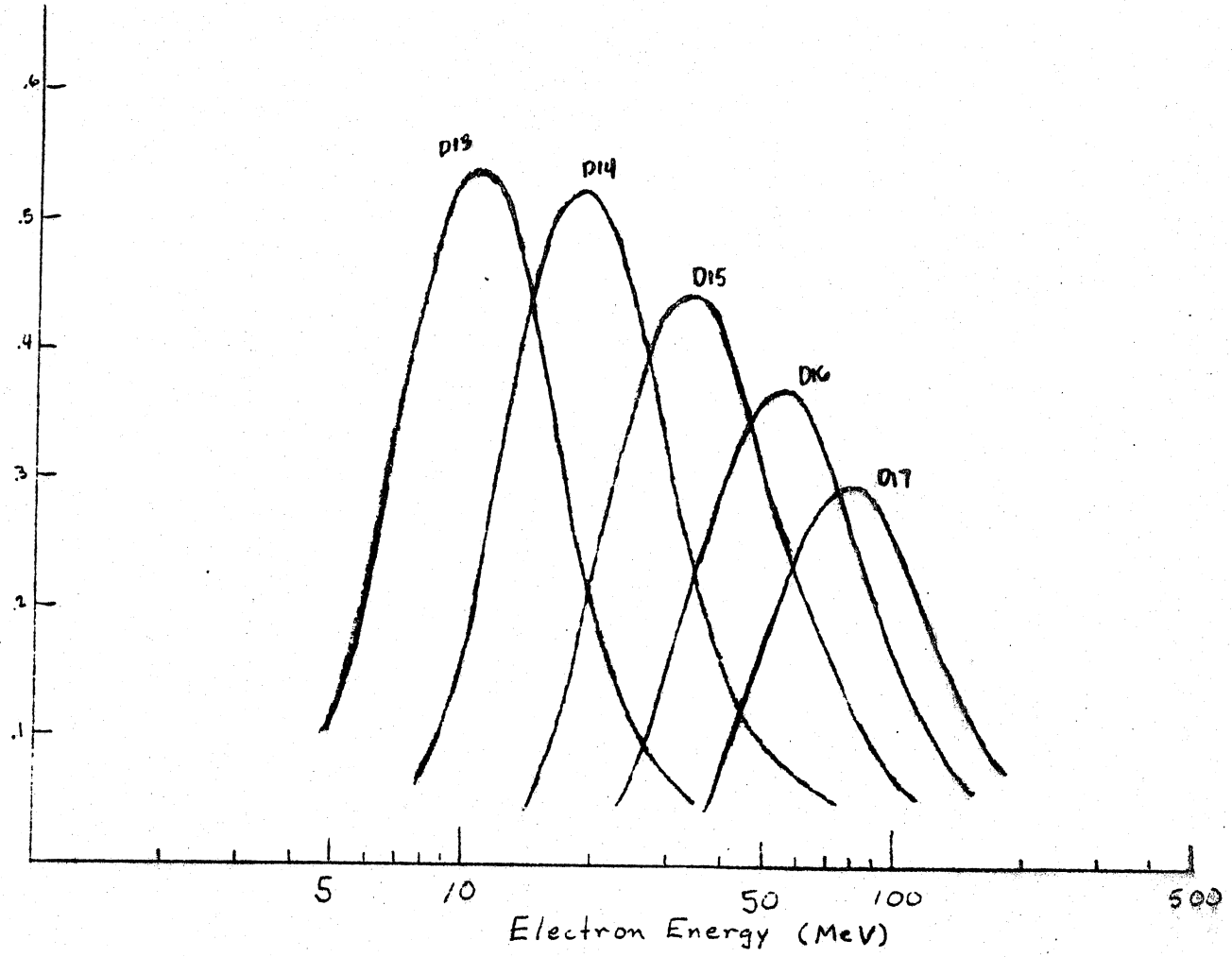

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4) Geometry Factors

Nominal geometry factors for the various ranges are given by the formula:

Geometry Factor = 0.5*PI**2[L**2 + 2*r**2 - L*SQRT(L**2 + 4*r**2)]
where r = 1.20 cm.

Range	L (cm)	Geometry Factor (cm**2-sr)
D12	2.00	3.12
D13	2.63	2.14
D14	3.26	1.53
D15	3.90	1.14
D16	4.58	0.86
D17	5.30	0.66

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Name	Accum Number	Subcom State (S1-S4)	Simplified Logic Equation	Description
TAN	R28	all	W1.W2.D3.D8*.G*	Electrons of appropriate range. See nominal response curves.
TLO	R29	even (S1=0)	TAN.D5.D6*.UT*	Low energy electrons.
THI	R29	odd (S1=1)	TAN.D7.UT* (D7 ^ D6)	High energy electrons.

TAN causes analysis. Events are stored in buffer called TET.

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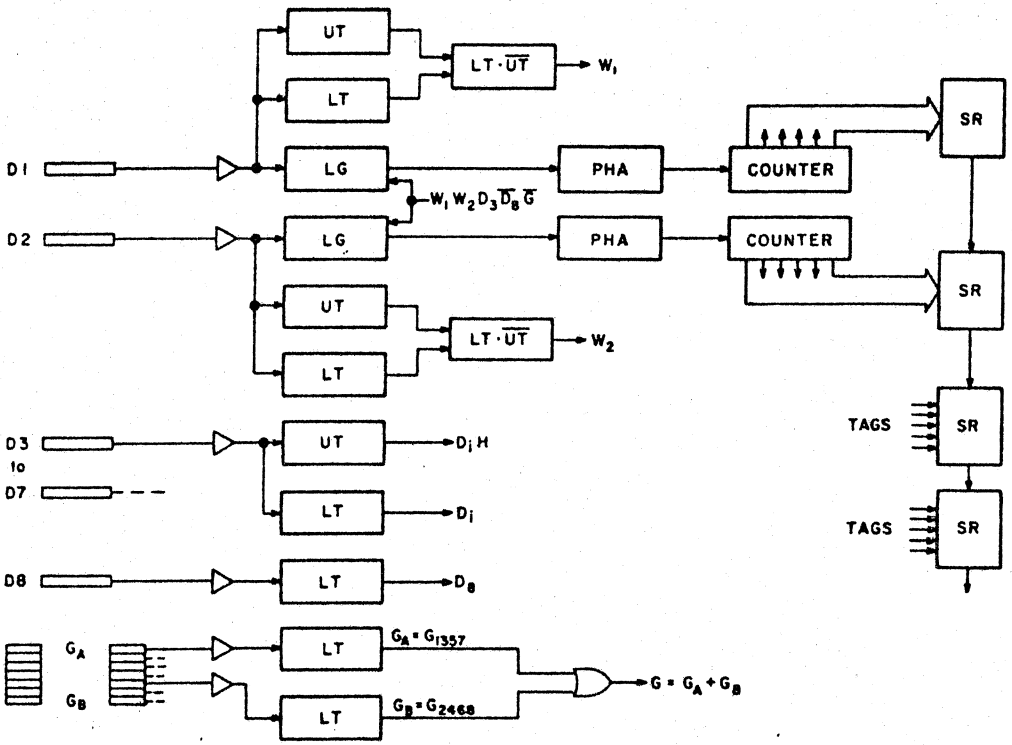

UT = UPPER THRESHOLD
LT = LOWER THRESHOLD

TET BLOCK DIAGRAM

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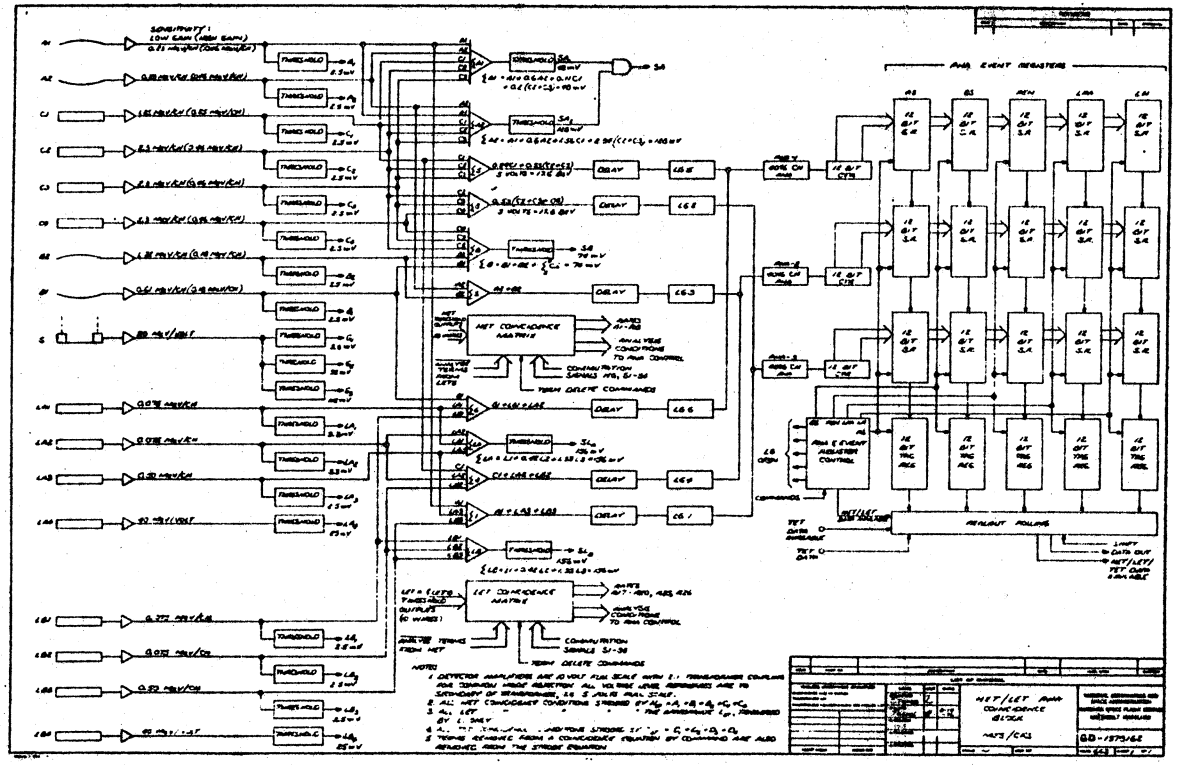

Rate commutator and cal stim block diagram available from DS or TG.
Need Data System Block Diagram.

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3 parallel redundant systems :

Block I :
- HET 1
- LET A
- LET B
- Rates 1 to 8, 17 to 20, 25
- Event Buffers for HET AS, HET BS, HET P, LET SL, LET SL*

Block II :
- HET 2
- LET C
- LET D
- Rates 9 to 16, 21 to 24, 26
- Event Buffers for HET AS, HET BS, HET P, LET SL, LET SL*

TET :
- TET
- Rates 28 to 30
- Event Buffer for TET

Blocks I and II are fully symmetrical. LET's A/B and C/D are fully symmetrical.

PHA Readout :

LET and HET

Sum	AS	BS	P	LET
A1 + LA3 + LB3	PHA3			PHA3
C2 + C3 + C4		PHA3	PHA3	
A2 + b2	PHA2	PHA2		
C1 + LA2 + LB2			PHA2	PHA2
C1 + C2 + C3	PHA1			
B1 + LA1 + LB1		PHA1	PHA1	PHA1

TET

D1	PHA1
D2	PHA2

Gain switching in HET is done with S5 after each 480 rate readouts when in AUTO mode.
High gain for S5 = 1

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Tag Bits :	1	2	3	4	5	6	7	8	9	10	11	12
HET AS	C1	C2	C3	C4	slant	G2*	G1.G3*	HG	0	0	block	caution
HET BS,PEN	C1	C2	C3	C4	slant	G2*	G1.G3*	HG	0	1	block	caution
LET A/B	slant	L3	L2	LB1	DLA2	DLB3	DLB2	DLA3	1	0	block=0	caution
LET C/D	slant	L3	L2	LD1	DLC2	DLD3	DLD2	DLC3	1	0	block=1	caution
TET (1)	D1L	D1H	D2L	D2H	D3L	D3H	D4L	D4H	1	1	0	caution
TET (2)	GA	GB	SD7/8	AD4L	D5L	D5H	D6L	D6H	D7L	D7H	D8L	GA + GB

Block = 0 for block I, 1 for Block II.

Caution flag = overflow in PHA or high gain/low gain switching in progress.

LET slants are ORed from 2 telescopes.

Polling:
Each event type is stored in a separate 48-bit register dedicated to that event type. Each block has 5 registers. The TET system has one register which may be sampled by either block. Between readouts, each block scans the event registers in the sequence LET SL*, LET SL, HET AS, HET BS, LET SL*, LET SL, HET PEN, TET, stopping only at a full register. A separate two-level polling device toggles alternately between blocks if both have data available, or selects data from the appropriate block if only one has data. If both blocks are empty, a null event is readout (48 0's).

Word format:

	1 12	13 24	25 36	37 48
HET/LET	TAG WORD	PHA3	PHA2	PHA1
TET	TAG WORD 1	TAG WORD 2	PHA2	PHA1

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Block I Analysis Equations

HET AS :
R1.LA3*.LB3*.SAS*.NAA*.BPHA*
low gain
A1.[A2].[C4*].[G3*].SA.[B2*].LA3*.LB3*.SAS*.NAA*.BPHA*
high gain
A1.[A2].[C4*].[G1*].G2*.[B2*].LA3*.LB3*.SAS*.NAA*.BPHA*

HET BS :
R2.LA1*.LB1*.SABp*.SABe*.NAB*.BPHA*
low gain
[B1].[B2].[C1*].[G3*].SB2.[A2*].LA1*.LB1*.NAB*.BPHA*
high gain
[B1].[B2].[C1*].[G1*].G2*.SB1.[A2*].LA1*.LB1*.NAB*.BPHA* if S1.S2 = 0
high gain
[B1].[B2].[C1*].[C4].[G1*].G2*.SB1*.[A2*].LA1*.LB1*.NAB*.BPHA* if S1.S2 = 1

HET PEN :
R3.LA1*.LA3*.LB1*.LB3*.SAP*.NAP*.BPHA*
[B1].[B2].[C1].LA1*.LA2*.LB1*.LB2*.SAP*.NAP*.BPHA*

LET SL* :
R17.SALA*.NALI*.BHET1*.BLETB*.BPHA* + R19.SALB*.NALI*.BHET1*.BLETA*.BPHA*
LA1.[LA2].[LA3].LA4*.SLA*.NALI*.BHET1*.BLETB*.BPHA*
+ LB1.[LB2].[LB3].LB4*.SLB*.SALB*.NALI*.BHET1*.BLETA*.BPHA*

LET SL :
R18.SALA*.NALII*.BHET1*.BLETB*.BPHA* + R20.SALB*.NALII*.BHET1*.BLETA*.BPHA*
LA1.[LA2].[LA3].LA4*.SLA.LSLA*.NALII*.BHET1*.BLETB*.BPHA*
+ LB1.[LB2].[LB3].LB4*.SLB.SALB*.NALII*.BHET1*.BLETA*.BPHA*

TET analysis Equations

TET
R28.BTET*.SAT*.NAT*
[D1L].[D1H*].[D2L].[D2H*].[D3L].(D4L + AD4L*).(D7L* + SD7/8*).(D8L* + SD7/8)
.[GA*].[GB*].BTET*.SAT*.NAT*

Definitions:

Command bits
SAS = Suppress AS mode
SABp = Suppress BSp mode
SABe = Suppress BSe mode
SAP = Suppress PEN mode
SALA = Suppress LET A
SALB = Suppress LET B
SAT = Suppress TET

Strobe signals
HST1 = HET 1 strobe = A1 + [B1] + [B2] + [C1] + [C4]
LSTA = LET A strobe = L1
LSTB = LET B strobe = LB1
TST = TET strobe = [D1L] + [D2L] + [D3L] + (D4L.AD4L)

Busy flags
BHET1 = A1 + B1 + C1
BLETA = LA1 + LA2 + LA3
BLETB = LB1 + LB2 + LB3
BPHA = busy PHA
NAA = AS register full
NAB = BS register full
NAT = TET register full
NALI = LET SL* register full
NALII = LET SL register full
BTET = TET PHA busy

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Rate definitions

```
R1 = ASZ3.HG1* + AS.HG1
   = A1.[A2].(SA + HG1).[C4*].([G1*].G2* + HG1*).([G3*] + HG1).[B2*].HST1
ASZ3 = A1.[A2].SA.[C4*].[G3*].[B2*].HST1
AS   = A1.[A2].[C4*].[G1*].G2*.[B2*].HST1

R2 = BSZ2.HG1* + BSp.(S1* + S2*).HG1 + BSe.(S1.S2).HG1
   = [B1].[B2].[C1*].([C4] + HG1* + S1* +S2*).(SB1 + HG1* + S1.S2).(SB1* + HG1* + S1* + S2*)
     .(SB2 + HG1).([G1*].G2* + HG1*).([G3*] + HG1).[A2*].HST1
BSZ2 = [B1].[B2].[C1*].SB2.[G3*].[A2*].HST1
BSp  = [B1].[B2].[C1*].SB1.[G1*].G2*.[A2*].HST1
BSe  = [B1].[B2].[C1*].[C4].SB1*.[G1*].G2*.[A2*].HST1

R3 = PEN = [B1].[B2].[C1].HST1

R4 = PEN.G1*

R5 = BS4Z2*.HG1*.S1 + BS4Z2.HG1*.S1* + BS4e.HG1.S1 + BS4p.HG1.S1*
   = [B1].[B2].C3*.[C4].G1*.(SB1* + HG1* + S1).(SB1 + HG1* + S1*).(SB2* + HG1 + S1).(SB2 + HG1 + S1*).HST1
BS4Z2* = [B1].[B2].C3*.[C4].G1*.SB2*
BS4Z2  = [B1].[B2].C3*.[C4].G1*.SB2
BS4e   = [B1].[B2].C3*.[C4].G1*.SB1*
BS4p   = [B1].[B2].C3*.[C4].G1*.SB1

R6 = BS3Z2*.HG1*.S1 + BS3Z2.HG1*.S1* + BS3e.HG1.S1 + BS3p.HG1.S1*
   = [B1].[B2].C2*.C3.[C4].G1*.(SB1* + HG1* + S1).(SB1 + HG1* + S1*).(SB2* + HG1 + S1).(SB2 + HG1 + S1*).HST1
BS3Z2* = [B1].[B2].C2*.C3.[C4].G1*.SB2*.HST1
BS3Z2  = [B1].[B2].C2*.C3.[C4].G1*.SB2.HST1
BS3e   = [B1].[B2].C2*.C3.[C4].G1*.SB1*.HST1
BS3p   = [B1].[B2].C2*.C3.[C4].G1*.SB1.HST1

R7 = BS2Z2*.HG1*.S1 + BS2Z2.HG1*.S1* + BS2e.HG1.S1 + BS2p.HG1.S1*
   = [B1].[B2].C2.C3.[C4].G1*.(SB1* + HG1* + S1).(SB1 + HG1* + S1*).(SB2* + HG1 + S1).(SB2 + HG1 + S1*).HST1
BS2Z2* = [B1].[B2].C2.C3.[C4].G1*.SB2*.HST1
BS2Z2  = [B1].[B2].C2.C3.[C4].G1*.SB2.HST1
BS2e   = [B1].[B2].C2.C3.[C4].G1*.SB1*.HST1
BS2p   = [B1].[B2].C2.C3.[C4].G1*.SB1.HST1
```

Where HG1 = high gain bit for HET 1, and other definitions are on the preceding page.

Approved _____ Date _____

Rate definitions

R8 = singles, as listed in the rate table.

R17 = LA1.[LA2].[LA3].LA4*.SLA*.LSTA

R18 = LA1.[LA2].[LA3].LA4*.SLA.LSTA

R19 = LB1.[LB2].[LB3].LB4*.SLB*.LSTB

R20 = LB1.[LB2].[LB3].LB4*.SLB.LSTB

R25 = Singles, etc. as listed in the rate.
LATRP = LA1.LA2.LA3.LA4*.LSTA
LBTRP = LB1.LB2.LB3.LB4*.LSTB

R27 is spare accumulator.

R28 = [D1L].[D1H*].[D2L].[D2H*].[D3L].(D4L + AD4L*).(D7L* + SD7/8*).(D8* + SD7/8).[GA*].[GB*].TST
= TAN

R29 = TLO.S1* + THI.S1
= [D1L].[D1H*].[D2L].[D2H*].[D3L].[D3H*].(D4L + AD4L*).D4H*.(D5L + S1).D5H*.(D6L* + S1).D6H*
.(D7L + S1* + SD7/8).(D7L* + S1* + SD7/8*).D7H*.(D8L* + S1*).[GA*].[GB*].TST
TLO = [D1L].[D1H*].[D2L].[D2H*].[D3L].[D3H*].(D4L + AD4L*)D4H*.D5L.D5H*.D6L*D6H*.D7H*.[GA*].[GB*].TST
THI = [D1L].[D1H*].[D2L].[D2H*].[D3L].[D3H*].(D4L + AD4L*).D4H*.D5H*.D6L.D6H*.(D7L + SD7/8).(D7L* + SD7/8*)
.D7H*.D8L*.[GA*].[GB*].TST

R30 = Singles, as listed in the rate table.

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Rate table

SB	R1	R2	R3	R4	R5	R6	R7	R8	R17	R18	R19	R20	R25	R28	R29	R30
0	ASZ3	BSZ2	PEN	PG	BS4Z2	BS3Z2	BS2Z2	A1	LAZ3*	LAZ3	LBZ3*	LBZ3	LA1	TAN	TLO	D6L
1	ASZ3	BSZ2	PEN	PG	BS4Z2*	BS3Z2*	BS2Z2*	A2	LAZ3*	LAZ3	LBZ3*	LBZ3	LA2	TAN	THI	GA + GB
2	ASZ3	BSZ2	PEN	PG	BS4Z2	BS3Z2	BS2Z2	C1	LAZ3*	LAZ3	LBZ3*	LBZ3	LA3	TAN	TLO	D5H
3	ASZ3	BSZ2	PEN	PG	BS4Z2*	BS3Z2*	BS2Z2*	C2	LAZ3*	LAZ3	LBZ3*	LBZ3	LA4	TAN	THI	D7L
4	ASZ3	BSZ2	PEN	PG	BS4Z2	BS3Z2	BS2Z2	B1	LAZ3*	LAZ3	LBZ3*	LBZ3	LASL	TAN	TLO	D6H
5	ASZ3	BSZ2	PEN	PG	BS4Z2*	BS3Z2*	BS2Z2*	SA1	LAZ3*	LAZ3	LBZ3*	LBZ3	LBSL	TAN	THI	D7H
6	ASZ3	BSZ2	PEN	PG	BS4Z2	BS3Z2	BS2Z2	SA2	LAZ3*	LAZ3	LBZ3*	LBZ3	LATRP	TAN	TLO	D5L
7	ASZ3	BSZ2	PEN	PG	BS4Z2*	BS3Z2*	BS2Z2*	SB	LAZ3*	LAZ3	LBZ3*	LBZ3	LBTRP	TAN	THI	D8L
8	ASZ3	BSZ2	PEN	PG	BS4Z2	BS3Z2	BS2Z2	C3	LAZ3*	LAZ3	LBZ3*	LBZ3	LB1	TAN	TLO	D1H
9	ASZ3	BSZ2	PEN	PG	BS4Z2*	BS3Z2*	BS2Z2*	C4	LAZ3*	LAZ3	LBZ3*	LBZ3	LB2	TAN	THI	D4H
10	ASZ3	BSZ2	PEN	PG	BS4Z2	BS3Z2	BS2Z2	B2	LAZ3*	LAZ3	LBZ3*	LBZ3	LB3	TAN	TLO	D2L
11	ASZ3	BSZ2	PEN	PG	BS4Z2*	BS3Z2*	BS2Z2*	G1	LAZ3*	LAZ3	LBZ3*	LBZ3	LB4	TAN	THI	D3L
12	ASZ3	BSZ2	PEN	PG	BS4Z2	BS3Z2	BS2Z2	B1	LAZ3*	LAZ3	LBZ3*	LBZ3	LASL	TAN	TLO	D1L
13	ASZ3	BSZ2	PEN	PG	BS4Z2*	BS3Z2*	BS2Z2*	SA1	LAZ3*	LAZ3	LBZ3*	LBZ3	LBSL	TAN	THI	D3H
14	ASZ3	BSZ2	PEN	PG	BS4Z2	BS3Z2	BS2Z2	SA2	LAZ3*	LAZ3	LBZ3*	LBZ3	LATRP	TAN	TLO	D2H
15	ASZ3	BSZ2	PEN	PG	BS4Z2*	BS3Z2*	BS2Z2*	SB	LAZ3*	LAZ3	LBZ3*	LBZ3	LBTRP	TAN	THI	D4L
16	AS	BSp	PEN	PG	BS4p	BS3p	BS2p	A1	LAZ3*	LAZ3	LBZ3*	LBZ3	LA1	TAN	TLO	D6L
17	AS	BSp	PEN	PG	BS4e	BS3e	BS2e	A2	LAZ3*	LAZ3	LBZ3*	LBZ3	LA2	TAN	THI	GA + GB
18	AS	BSp	PEN	PG	BS4p	BS3p	BS2p	C1	LAZ3*	LAZ3	LBZ3*	LBZ3	LA3	TAN	TLO	D5H
19	AS	BSe	PEN	PG	BS4e	BS3e	BS2e	C2	LAZ3*	LAZ3	LBZ3*	LBZ3	LA4	TAN	THI	D7L
20	AS	BSp	PEN	PG	BS4p	BS3p	BS2p	B1	LAZ3*	LAZ3	LBZ3*	LBZ3	LASL	TAN	TLO	D6H
21	AS	BSp	PEN	PG	BS4e	BS3e	BS2e	SA1	LAZ3*	LAZ3	LBZ3*	LBZ3	LBSL	TAN	THI	D7H
22	AS	BSp	PEN	PG	BS4p	BS3p	BS2p	SA2	LAZ3*	LAZ3	LBZ3*	LBZ3	LATRP	TAN	TLO	D5L
23	AS	BSe	PEN	PG	BS4e	BS3e	BS2e	SB	LAZ3*	LAZ3	LBZ3*	LBZ3	LBTRP	TAN	THI	D8L
24	AS	BSp	PEN	PG	BS4p	BS3p	BS2p	C3	LAZ3*	LAZ3	LBZ3*	LBZ3	LB1	TAN	TLO	D1H
25	AS	BSp	PEN	PG	BS4e	BS3e	BS2e	C4	LAZ3*	LAZ3	LBZ3*	LBZ3	LB2	TAN	THI	D4H
26	AS	BSp	PEN	PG	BS4p	BS3p	BS2p	B2	LAZ3*	LAZ3	LBZ3*	LBZ3	LB3	TAN	TLO	D2L
27	AS	BSe	PEN	PG	BS4e	BS3e	BS2e	G1	LAZ3*	LAZ3	LBZ3*	LBZ3	LB4	TAN	THI	D3L
28	AS	BSp	PEN	PG	BS4p	BS3p	BS2p	B1	LAZ3*	LAZ3	LBZ3*	LBZ3	LASL	TAN	TLO	D1L
29	AS	BSp	PEN	PG	BS4e	BS3e	BS2e	SA1	LAZ3*	LAZ3	LBZ3*	LBZ3	LBSL	TAN	THI	D3H
30	AS	BSp	PEN	PG	BS4p	BS3p	BS2p	SA2	LAZ3*	LAZ3	LBZ3*	LBZ3	LATRP	TAN	TLO	D2H
31	AS	BSe	PEN	PG	BS4e	BS3e	BS2e	SB	LAZ3*	LAZ3	LBZ3*	LBZ3	LBTRP	TAN	THI	D4L

SB = Subcom state = S1 + 2.S2 + 4.S3 +8.S4 + 16.S5 S5 = HG
Rate table is for AUTO mode. When CRS is commanded to HG or HG* mode only the bottom or top half is read out.
Note that there are actually two high gain bits.

Approved _____ Date _____

subcom state	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
rate accum																
1	AS	AS	AS	AS	AS	AS	AS	AS	AS	AS	AS	AS	AS	AS	AS	AS
2	BSp	BSp	BSp	BSe	BSp	BSp	BSp	BSe	BSp	BSp	BSp	BSe	BSp	BSp	BSp	BSe
3	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN
4	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG
5	BS4p	BS4e	BS4p	BS4e	BS4p	BS4e	BS4p	BS4e	BS4p	BS4e	BS4p	BS4e	BS4p	BS4e	BS4p	BS4e
6	BS3p	BS3e	BS3p	BS3e	BS3p	BS3e	BS3p	BS3e	BS3p	BS3e	BS3p	BS3e	BS3p	BS3e	BS3p	BS3e
7	BS2p	BS2e	BS2p	BS2e	BS2p	BS2e	BS2p	BS2e	BS2p	BS2e	BS2p	BS2e	BS2p	BS2e	BS2p	BS2e
8	A1	A2	C1	C2	B1	SA1	SA2	SB	C3	C4	B2	G1	B1	SA1	SA2	SB
9	AS	AS	AS	AS	AS	AS	AS	AS	AS	AS	AS	AS	AS	AS	AS	AS
10	BSp	BSp	BSp	BSe	BSp	BSp	BSp	BSe	BSp	BSp	BSp	BSe	BSp	BSp	BSp	BSe
11	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN
12	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG
13	BS4p	BS4e	BS4p	BS4e	BS4p	BS4e	BS4p	BS4e	BS4p	BS4e	BS4p	BS4e	BS4p	BS4e	BS4p	BS4e
14	BS3p	BS3e	BS3p	BS3e	BS3p	BS3e	BS3p	BS3e	BS3p	BS3e	BS3p	BS3e	BS3p	BS3e	BS3p	BS3e
15	BS2p	BS2e	BS2p	BS2e	BS2p	BS2e	BS2p	BS2e	BS2p	BS2e	BS2p	BS2e	BS2p	BS2e	BS2p	BS2e
16	A1	A2	C1	C2	B1	SA1	SA2	SB	C3	C4	B2	G1	B1	SA1	SA2	SB
17	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*
18	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3
19	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*
20	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3
21	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*
22	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3
23	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*
24	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3
25	LA1	LA2	LA3	LA4	LASL	LBSL	LATRP	LBTRP	LB1	LB2	LB3	LB4	LASL	LBSL	LATRP	LBTRP
26	LC1	LC2	LC3	LC4	LCSL	LDSL	LCTRP	LDTRP	LD1	LD2	LD3	LD4	LCSL	LDSL	LCTRP	LDTRP
27																
28	TAN	TAN	TAN	TAN	TAN	TAN	TAN	TAN	TAN	TAN	TAN	TAN	TAN	TAN	TAN	TAN
29	TLO	THI	TLO	THI	TLO	THI	TLO	THI	TLO	THI	TLO	THI	TLO	THI	TLO	THI
30	D6L	GA+GB	D5H	D7L	D6H	D7H	D5L	D8L	D1H	D4H	D2L	D3L	D1L	D3H	D2H	D4L

Approved _____ Date _____

subcom state	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
rate accum																
1	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3
2	BSZ2	BSZ2	BSZ2	BSZ2	BSZ2	BSZ2	BSZ2	BSZ2	BSZ2	BSZ2	BSZ2	BSZ2	BSZ2	BSZ2	BSZ2	BSZ2
3	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN
4	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG
5	BS4Z2	BS4Z2*	BS4Z2	BS4Z2*	BS4Z2	BS4Z2*	BS4Z2	BS4Z2*	BS4Z2	BS4Z2*	BS4Z2	BS4Z2*	BS4Z2	BS4Z2*	BS4Z2	BS4Z2*
6	BS3Z2	BS3Z2*	BS3Z2	BS3Z2*	BS3Z2	BS3Z2*	BS3Z2	BS3Z2*	BS3Z2	BS3Z2*	BS3Z2	BS3Z2*	BS3Z2	BS3Z2*	BS3Z2	BS3Z2*
7	BS2Z2	BS2Z2*	BS2Z2	BS2Z2*	BS2Z2	BS2Z2*	BS2Z2	BS2Z2*	BS2Z2	BS2Z2*	BS2Z2	BS2Z2*	BS2Z2	BS2Z2*	BS2Z2	BS2Z2*
8	A1	A2	C1	C2	B1	SA1	SA2	SB	C3	C4	B2	G1	B1	SA1	SA2	SB
9	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3	ASZ3
10	BSZ10	BSZ10	BSZ10	BSZ10	BSZ10	BSZ10	BSZ10	BSZ10	BSZ10	BSZ10	BSZ10	BSZ10	BSZ10	BSZ10	BSZ10	BSZ10
11	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN	PEN
12	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG	PG
13	BS4Z2	BS4Z2*	BS4Z2	BS4Z2*	BS4Z2	BS4Z2*	BS4Z2	BS4Z2*	BS4Z2	BS4Z2*	BS4Z2	BS4Z2*	BS4Z2	BS4Z2*	BS4Z2	BS4Z2*
14	BS3Z2	BS3Z2*	BS3Z2	BS3Z2*	BS3Z2	BS3Z2*	BS3Z2	BS3Z2*	BS3Z2	BS3Z2*	BS3Z2	BS3Z2*	BS3Z2	BS3Z2*	BS3Z2	BS3Z2*
15	BS2Z2	BS2Z2*	BS2Z2	BS2Z2*	BS2Z2	BS2Z2*	BS2Z2	BS2Z2*	BS2Z2	BS2Z2*	BS2Z2	BS2Z2*	BS2Z2	BS2Z2*	BS2Z2	BS2Z2*
16	A1	A2	C1	C2	B1	SA1	SA2	SB	C3	C4	B2	G1	B1	SA1	SA2	SB
17	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*	LAZ3*
18	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3	LAZ3
19	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*	LBZ3*
20	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3	LBZ3
21	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*	LCZ3*
22	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3	LCZ3
23	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*	LDZ3*
24	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3	LDZ3
25	LA1	LA2	LA3	LA4	LASL	LBSL	LATRP	LBTRP	LB1	LB2	LB3	LB4	LASL	LBSL	LATRP	LBTRP
26	LC1	LC2	LC3	LC4	LCSL	LDSL	LCTRP	LDTRP	LD1	LD2	LD3	LD4	LCSL	LDSL	LCTRP	LDTRP
27																
28	TAN	TAN	TAN	TAN	TAN	TAN	TAN	TAN	TAN	TAN	TAN	TAN	TAN	TAN	TAN	TAN
29	TLO	THI	TLO	THI	TLO	THI	TLO	THI	TLO	THI	TLO	THI	TLO	THI	TLO	THI
30	D6L	GA+GP	D5H	D7L	D6H	D7H	D5L	D8L	D1H	D4H	D2L	D3L	D1L	D3H	D2H	D4L

Approved _____ Date _____

Each 12-bit serial command consists of a 4-bit address code specifying a subsystem or device to be controlled, and 8 command data bits. Bit number 1 is the first bit transmitted, and is the MSB of the address code.

```
bit :   1   2   3   4 | 5   6   7   8   9   10  12
                      |
          address     |           data
```

Address	Use in command and/or status
0	Status readout of some miscellaneous control bits
1	HET 1 preamps
2	HET 2 preamps
3	LET A/B preamps
4	LET C/D preamps
5	Block I PHA control
6	Block II PHA control
7	Block I analysis control
8	Block II analysis control
9	unused
10	TET control
11	TET preamps
12	HET C preamps
13	Miscellaneous control
14	unused
15	unused

Status readout pattern duplicates commands exactly except for addresses 0 and 10. Address 0 is for status readout only. Address 10 has different bit order for command and status. See command/status table.

Approved _____ Date _____

Command/status table

	0	1/2	3/4	5/6	7/8	cmnd 10	stat 10	11	12	13
5	redundant polling indicator	A1 power off	LA1 power off	Delete LA3 terms	Delete LB3 terms	Disable TET	Add D4 terms	D1 power off	H1C1 power off	High Volt redundant enable
6		A2 power off	LA2 power off	Delete LA2 terms	Delete LB2 terms	Delete W1 terms	Disable TET	D2 power off	H1C2 power off	Cal Stim disable
7	High Volt enable indicator	B1 power off	LA3 power off	Disable H1P mode	Delete G* terms	Delete D3 terms	Delete GB* terms	D3 power off	H1C3 power off	redundant polling
8	HET 2 high gain indicator	B2 power off	LA4 power off	Disable H1BSp mode	Delete C4 terms	Subs D7L* for D8*	Delete GA* terms	D4 power off	H1C4 power off	
9	HET 1 high gain indicator	C1 Guard power off	LB1 power off	Disable H1BSe mode	Delete C1 terms	Delete W2 terms	Subs D7L* for D8*	D5 power off	H2C1 off	H1 Gain auto
10	Cal Stats Q3 (MSB)	C2 Guard power off	LB2 power off	Disable H1AS mode	Delete B2 terms	Delete GB* terms	Delete D3 terms	D6 power off	H2C2 power off	H1 Gain set high
11	Cal Stats Q2	C3 Guard power off	LB3 power off	Disable LET F	Delete B1 terms	Delete GA* terms	Delete W1 terms	D7 power off	H2C3 off	H2 Gain auto
12	Cal Stats Q1 (LSB)	C4 Guard power off	LB4 power off	Disable LET A	Delete A2 terms	Add D4 terms	Delete W2 terms	D8 power off	H2C4 power off	H2 Gain set high

Approved _____ Date _____

The cal sequence begins at the start of the first complete rate commutator cycle following receipt of the cal command. The sequence lasts for 8 complete commutator cycles (i.e. 8 x 16 x 30 = 3840 rate words, about 12.5 minutes at normal data rates) and turns off automatically. Data will not appear in telemetry until completion of the first accumulation interval within the commutator cycle (delay is 8 second minimum, 104 second maximum). HET, LET, and TET test pulses do not occur simultaneously but are separated by about 70 microseconds. Each occurs at a repetition rate of 3.6 kHz. There are a total of 10 separate cal busses which are pulsed separately and in combination, as shown in the table below. Coincidence rates stimulated are also listed; not shown are the appropriate singles in R8, R9, R25, R26, and R30. The rates which are not stimulated by this cal sequence are R7, R16, R17, R19, R21, and R23. Of these the last four (LET's without slants) can be stimulated by turning off the L3 preamps and disabling the L3 terms in the coincidence system.

cal busses on during cal period

cal bus	detectors	LG 1	HG 2	LG 3	HG 4	LG 5	HG 6	LG 7	HG 8
LET I CAL A	A1, A2, C1, C3, SA		X		X				
HET I CAL B	B1, B2, C4			X	X				
HET II CAL A	A1, A2, C1, C3, SA						X		X
HET II CAL B	B1, B2, C4							X	X
TET CAL A	D1, D2, D3, D4, D5		X		X		X		X
TET CAL B	D6, D7			X	X			X	X
LET A CAL	L1, L2, L3, SL	X					X	X	X
LET B CAL	L1, L2, L3, SL		X			X		X	X
LET C CAL	L1, L2, L3, SL			X		X	X		X
LET D CAL	L1, L2, L3, SL				X	X	X	X	
	rates stimulated	R18 R25	R1 R20 R25 R28 R29	R2 R5 R22 R26	R3 R4 R6 R24 R26 R28 R29	R20 R22 R24 R25 R26	R9 R18 R22 R24 R25 R26 R28 R29	R10 R13 R18 R20 R24 R25 R26	R11 R12 R14 R18 R20 R22 R25 R26 R28 R29

Approved _____ Date _____

6) Analog Multiplexer Data

The CRS will internally multiplex 24 analog measurements onto a single CRS-FDS analog line. The multiplexer will be controlled by a simple modulo-24 counter which is advanced once by each two signals on the CRS-FDS Analog Mux Step line. The multiplexer is reset by a signal on the CRS-FDS Analog Mux Reset line. The 24 parameters to be sampled are:

no.	name	description
1	v(+10)	+ 10 volt power supply voltage
2		
3	V(+6)	+ 6 volt "
4	V(+3)	+ 3 volt "
5	V(-3)	- 3 volt "
6	V(-6)	- 6 volt "
7	V(-12)	- 12 volt power supply voltage
8		
9		
10	TLA	LET A temperature
11	TLB	LET B temperature
12	TLC	LET C temperature
13	TLD	LET D temperature
14	THA	HET 1 temperature
15	THB	HET 2 temperature
16	TTT	TET temperature
17	TPC	Power converter temperature
18	TBP	Baseplate temperature
19	TPHA	PHA electronics temperature
20	TH2	HET2(left) side heater temperature
21	TH1	HET1(right) side heater temperature
22		
23		
24		

Approved _____ Date _____

1) Spacecraft Mechanical Configuration

Separate attachment.

Approved _____ Date _____

2) Telescope Pointing Vectors

Approved _____ Date _____